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Contact Information

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Research Interests

Broad interests in robust computer system design with emphasis on efficiency and performance in various system stack abstraction layers, from computer architecture to operating systems and programming languages.

Education

July 2013 (expected): **Ph.D.,** Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, USA
Thesis: *"Lightweight and low-cost mechanisms to enable parallel monitoring of multithreaded applications"* Advisor: Prof. Babak Falsafi

May 2011: ***M.Sc.,*** Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, USA
Advisor: Prof. Babak Falsafi

June 2006: *M.Sc.* Department of Computer Science, University of Crete, Greece. Thesis: *"Design and implementation of* ***a coherent memory system, including a coherent network interface, for a Power PC processor on a Xilinx Virtex II Pro FPGA"***
Advisor: Prof. Manolis Katevenis

June 2004: **B.Sc.** Department of Computer Science, University of Crete, Greece. Thesis: *"Study of Asynchronous Latch Controllers for desynchronized systems"*
Advisors: Dr. Christos Sotiriou, Prof. Manolis Katevenis

Honors

- December 2011 — Graduate fellowship awarded to Greek students with exceptional academic performance (Gerondelis Foundation, MA)
- June 2009 — August 2009: Summer Research Fellowship (Intel Labs Pittsburgh, PA)
- June 2008 — August 2008: Summer Research Fellowship (Intel Labs Pittsburgh, PA)
- September 2004 —July 2006: ICS-FORTH graduate fellowship (Greece)
- May 2003 — August 2004: ICS-FORTH undergraduate fellowship (Greece)

Professional Experience

September 2006— Present: Graduate Research Assistant, Carnegie Mellon University *June 2007 — August 2007:* Intern, Intel Research Pittsburgh.

Mentors: Dr. Michael A. Kozuch and Dr. Shimin Chen.

May 2003 —June 2006: Research Assistant, Institute of Computer Science — Foundation for Research and Technology Hellas (ICS-FORTH)

Referred Conference and Journal Publications

1. **ParaLog: Enabling and Accelerating Online Parallel Monitoring of Multithreaded Applications.** [redacted], Michelle L. Goodstein, Michael A. Kozuch, Shimin Chen, Babak Falsafi, Phillip B.

Gibbons, and Todd C. Mowry. *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2010.*

2. **Butterfly Analysis: Adapting Dataflow Analysis to Dynamic Parallel Monitoring.** Michelle L. Goodstein, [redacted] Shimin Chen, Phillip B. Gibbons, Michael A. Kozuch, Todd C. Mowry. *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2010.*
3. **Flexible Hardware Acceleration for Instruction-Grain Lifeguards.** Shimin Chen, Michael A. Kozuch, Phillip B. Gibbons, Michael Ryan, Theodoros Strigkos, Todd C. Mowry, Olatunji Ruwase, [redacted] Babak Falsafi, Vijaya Ramachandran. *IEEE Micro, Jan/Feb 2009 Special Issue: Micro's Top Picks in Computer Architecture Conferences.*
4. **Flexible Hardware Acceleration for Instruction-Grain Program Monitoring.** Shimin Chen, Michael A. Kozuch, Theodoros Strigkos, Babak Falsafi, Phillip B. Gibbons, Todd C. Mowry, Vijaya Ramachandran, Olatunji Ruwase, Michael Ryan and [redacted] *International Symposium on Computer Architecture (ISCA), June 2008.*

Under Submission

5. Resolve: Enabling Accurate Parallel Monitoring under Relaxed Memory Models. [redacted] Sotiria Fytraki, Michael A. Kozuch, Phillip B. Gibbons and Babak Falsafi. *Under submission.*

6. MonArch: A Flexible Single-Core Monitoring Architecture.
Sotiria Fytraki, [redacted] Onur Kocberber, Boris Grot and Babak Falsafi. *Under submission.*

Workshop Publications, Technical Reports and Demo Presentations

7. Parallel LBA: Coherence-based Parallel Monitoring of Multithreaded Applications. [redacted] Michelle Goodstein, Michael A. Kozuch, Shimin Chen, Babak Falsafi, Phillip B. Gibbons, Todd C. Mowry, and Olatunji Ruwase. *Carnegie Mellon University Technical Report: CMU-CS-09-108, March 2009*

8. The Butterfly Model: Theoretical Foundations.
Michelle Goodstein, [redacted] Shimin Chen, Phillip Gibbons, Michael A. Kozuch, and Todd C. Mowry. *Carnegie Mellon University Technical Report: CMU-CS08-170, February 2009.*

9 Log-Based Architectures: General-Purpose Program Monitoring Using Idle Cores. Shimin Chen, Babak Falsafi, Phillip B. Gibbons, Michael A. Kozuch, Todd C. Mowry, Michael Ryan, Radu Teodorescu, Anastasia Ailamaki, Limor Fix, Gregory. R. Ganger, Bin Lin, Olatunji Ruwase, Theodoros Strigkos and [redacted] *Intel Research Pittsburgh Tech Report TRP-08-02*

10. **An FPGA-based Prototyping Platform for Research in High-Speed Interprocessor Communication.**
Vassilis Papaefstathiou, Giorgos Kalokairinos, Aggelos Ioannou, Michael Papamichael, Giorgos Mihelogiannakis, Stamatis Kavadias, [redacted] Dionisios Pnevmatikatos and Manolis Katevenis. *2nd HIPEAC Industrial Workshop, October 2006.*
11. **An Asynchronous Open-Source DLX Processor.**
Nikolaos Andrikos, Evriklis Kounalakis, Pavlos M. Mattheakis, Christos P. Sotiriou and [redacted] *Demo presented in ASYNC 2004.*

Research Experience

My Ph.D. thesis work focused on hardware and software techniques that target software robustness through instruction-grain monitoring of program execution. Specifically, I studied the challenges of parallel instruction-grain monitoring for multithreaded applications. Parallel monitoring of multithreaded applications requires (i) proper coordination of monitoring tasks in order to correctly process concurrent application events and (ii) correct and efficient synchronization mechanisms to ensure atomicity of shared monitoring state. My thesis work addressed these challenges by introducing novel hardware- and software-based mechanisms, enabling accurate and efficient parallel monitoring and making it applicable to a wide range of architectures [1, 5].

September 2006 - Present:	Research Assistant, Carnegie Mellon University, Pittsburgh USA. Log-Based Architectures Group (LBA) (http://www.cs.cmu.edut'lba).

- Current work: Explore hardware-assisted acceleration mechanisms that reduce the runtime and energy overhead of monitoring multithreaded applications.
- Extended *ParaLog's* applicability [1], by introducing software mechanisms to support monitoring under less strict memory models, such as SPARC's RMO (work under submission [5]).
- Designed and evaluated novel mechanisms, based on tracking cache coherence activity, to enable efficient and accurate parallel monitoring of multithreaded applications under the Sequential Consistency and Total Store Order memory models [1].
- Contributed to the development of *Butterfly Analysis [2];* a novel monitoring approach that uses dataflow analysis to monitor parallel applications. Took part in defining the microarchitectural requirements and provided infrastructure support.
- Contributed to the initial papers of my group [3, 4]; designed and evaluated the hardware compression mechanisms that communicate application's execution trace from the application to the monitoring core.

September 2011— Visiting Ph.D. student at EPFL, Lausanne, Switzerland.
Present: Parallel Systems Architecture Lab (PARSA) (http://parsa.epfl.ch).

- Contributed to the development of *IVIonArch [6];* a novel monitoring architecture that mitigates the high runtime and resource overhead of monitoring frameworks. I participated in all the stages of this work: identifying the opportunity for filtering out redundant monitoring activity, defining the required hardware and software mechanisms, developing the infrastructure and evaluating the monitoring architecture.

February 2005— Research Assistant, University of Crete and ICS-FORTH, Greece.
June 2006: Packet Switch Architecture Group (http://www.ics.forth.gr/carv).

- Designed and implemented a coherent memory system with a coherent network interface, for a Power PC processor on a Xilinx Virtex II Pro FPGA [10].

May 2003— Research Assistant, University of Crete and ICS-FORTH, Greece.
February 2005: Asynchronous Circuits and Systems (http://www.ics.forth.gr/carv).

- Evaluated the performance characteristics of previously proposed handshake protocols adopted by latch controllers in asynchronous systems (BSc thesis).
- Contributed to the implementation of the de-synchronized version of the DLX processor and to the effort of porting it on to a Xilinx Spartan-2E FPGA (ASPIDA project). This effort was presented as a demo in ASYNC 2004 [11].
- Contributed to the back-end of the ASIC implementation of the de-synchronized DLX system SOC (verification and place and route).

Teaching Experience

Teaching Assistant for the following courses:

- 15-740/18-740 Computer Architecture (Fall 2010), Carnegie Mellon University
  - Held TA hours, prepared class assignments, identified class projects and advised students on their projects, graded assignments and exams.
- 18-741 Advanced Computer Architecture (Spring 2009), Carnegie Mellon University
  - Held TA hours, prepared class assignments, identified class projects and advised students on their projects, graded assignments and exams.
- CS-325 Embedded Systems Lab (Spring 2006), University of Crete
  - Held TA hours and lab sessions, prepare class assignments, graded assignments and exams.
- CS-220 Digital Design Laboratory (Spring and Fall 2005), University of Crete
  - Held TA hours and lab sessions, prepared class assignments, graded assignments and exams.
- CS-422 Introduction to VLSI systems (Fall 2004), University of Crete
  - Held TA hours, prepared class assignments, graded assignments and exams.

Grants

- Co-author of "At-Speed Program Monitoring (almost) for Free", PI Babak Falsafi. Swiss National Science Foundation, 163K CHF ($174K USD), EPFL, Duration: 2012 — 2015.

External Reviewer

- HPCA 2010, DATE 2011, MSPC 2013

Technical Skills

- Programming or scripting languages: C/C++, SPARC and x86 assembly, bash

Operating Systems: Linux, Solaris, Windows

- Cycle-accurate simulation: Flexus (http://parsa.epfl.ch/simflex/index.html)
- Functional full-system simulators: Wind River Simics
- Hardware description languages: Verilog
- Hardware design flow tools: Xilinx ISE and EDK, Synopsis Design Compiler

Software Developed/Maintained:

- Flexus Simulator: a scalable, full system, cycle accurate simulator of multicore and multiprocessor systems based on Virtutech Simics. During my studies at CMU, I was responsible for maintaining, distributing and providing support for the Flexus codebase (www.ece.cmu.edu/'slmflex). Flexus is written in C++, makes extensive use of the Boost library and comprises of 300K lines of code, approximately.

- Project simulator: I was the main developer of the project simulator used during my studies. The simulator is based on Virtutech Simics and extends Flexus to enable cycle-accurate simulation of a multicore system with monitoring capabilities (i.e., capturing information for all monitored instructions and dispatching handlers to examine each instruction).